REMARKS

This paper is being provided in response to the May 5, 2003 Final Office Action for the above-referenced application. In this response, Applicants have cancelled claim 2 and amended claims 1, 3-5, 7 and 8 to clarify that which Applicants deem to be the invention. Applicants respectfully submit that the modifications to the claims are all supported by the originally filed application.

The rejection of claims 4 and 5 under 35 U.S.C. 112, second paragraph has been addressed by amendments to those claims provided herein in accordance with the guidelines provided in the Office Action. Accordingly, Applicants respectfully request that this rejection be withdrawn.

The rejection of Claims 1 and 8-19 under 35 U.S.C. 102(e) as being anticipated by Yamamoto et al. (U.S. Patent No. 6,408,370) is hereby traversed and reconsideration thereof is respectfully requested. Applicants respectfully submit that Claims 1 and 8-19 are patentable over Yamamoto, for reasons set forth in detail below.

Claim 1, as amended herein, recites a data storage system that includes a first disk drive unit, a second disk drive unit, coupled to the first disk drive unit by a bus, a main cache memory, coupled to the bus, that caches data from both the first disk drive unit and the second disk drive unit, and a secondary memory separate from the main cache memory and provided as part of the first disk drive unit, wherein the secondary memory has at least two sections, a first section used by the first disk drive unit to facilitate disk

accesses and a second section used to cache data provided to the second section from the second disk drive unit while said main cache memory caches data from both the first disk drive unit and the second disk drive unit.

Claim 8, as amended herein, recites a data storage system that includes a first disk drive including a section of onboard memory associated with the first disk drive and including an interface that handles data communication to and from the first disk drive, a second disk drive that provides data to the first disk drive via the interface, a main cache memory that caches data from both the first and second disk drives, the main cache memory being separate from the first and second disk drives and separate from the onboard memory, and memory that caches data of the data storage system, the memory including the section of onboard memory associated with the first disk drive where the section includes a portion of data cached from at least the second disk drive and wherein data from the second disk drive is provided to the onboard memory. Claims 9-19 depend from claim 8.

Yamamoto discloses dual writing of data through the effect of two controllers. (Col. 1, Lines 6-7). Yamamoto's Figure 1 illustrates a general configuration that includes a primary controller 104 connected to one or more disk units 105 and a secondary controller 109 connected to one or more disk units 105. The primary controller includes a control memory 107 and a cache memory 108 that are non-volatized. A processor 100 provides data to the primary controller 104. The primary controller 104 provides a function to transfer data to the secondary controller 109. (Col. 1, Lines 56-58). The write

data managing information 113 corresponding to the write data record 112 is created on the control memory 107. (Col. 3, Line 65-Col. 4, Line 5). At first, the received write data 112 is stored in the cache memory 108. The primary controller then transmits the write data to the secondary controller 109 which subsequently transfers the data to one of the disk units 105 coupled thereto.

Yamamoto generally discloses a system where data flows from the processor 100 to the primary controller 104 (and memory units thereof 107, 108) and from the primary controller 104 to the secondary controller 109. The controllers 104, 109 write data to the specific disk units 105 coupled thereto. However, Applicants respectfully submit that there is no memory of Yamamoto that can be fairly characterized as a main cache memory separate from both disk drives that caches data for both disk drives while there is a secondary memory (claim 1) or onboard memory (claim 8) that is part of the first disk drive that caches data for both the first and second disk drives.

In view of the foregoing, Applicants respectfully submits that Yamamoto neither discloses, teaches, or suggests Applicants' Claims 1 and 8-19 and request that the rejection be reconsidered and withdrawn.

The rejection of claim 2 as being anticipated by DeKoning has been made moot by cancellation of claim 2 herein.

The rejection of Claims 3-7 under 35 U.S.C. 103(a) as being unpatentable over Yamamoto is hereby traversed and reconsideration thereof is respectfully requested in view of amendments to the claims contained herein.

Applicants' Claim 3, as amended herein, recites a data storage device that includes a first section of onboard volatile memory containing data for the storage device, an interface for communicating data from the data storage device to a main cache memory, where the main cache memory contains data from at least one other data storage device and where the main cache memory is separate from the data storage device and the at least one other data storage device, and a second section of onboard volatile memory associated with the data storage device and used as a cache including data cached from the at least one other data storage device, wherein the second section of onboard volatile memory is provided with data from the at least one other data storage device. Claims 4-7 depend from claim 3.

Yamamoto is summarized above.

For reasons similar to those set forth above regarding independent Claim 1, Applicants' Claim 3 is neither disclosed nor suggested by the Yamamoto in that the Yamamoto neither discloses nor suggests a memory (or any interface thereto as recited in claim 3) that can be fairly characterized as a main cache memory separate from the storage device and an other storage device that caches data for both storage devices while

there is an onboard memory that is part of the storage device that caches data for both of the storage devices.

In view of the foregoing, Applicants respectfully submits that Yamamoto neither discloses, teaches, or suggests Applicants' Claims 3-7 and thus applicants respectfully request that the rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
CHOATE, HALL & STEWART

July 2, 2003
Date

Donald W. Muirhead
Reg. No. 33,978

Choate, Hall & Stewart
Patent Group
Exchange Place
53 State Street
Boston, MA 02109-2804